CLAIMS

1. A router, comprising:

a content addressable memory which stores Internet Protocol address prefixes in an order independent of lengths of the Internet Protocol address prefixes; and

an encoder coupled to the content addressable memory which stores a plurality of codes, corresponding to the Internet Protocol address prefixes in the content addressable memory, and compares the codes corresponding to matching Internet Protocol address prefixes to find a longest matching Internet Protocol address prefix.

2. The router of claim 1, further comprising:

a memory coupled to the encoder, the memory for storing a port number corresponding to each Internet Protocol address prefix in the content addressable memory and other information for routing an incoming Internet Protocol packet.

3. The router of claim 1, wherein the encoder includes circuitry for finding one of the plurality of codes.

4. The router for claim 1, wherein the encoder includes circuitry for deleting one of the plurality of codes.

5. The router of claim 1, wherein each of the plurality of codes indicates a number of relevant bits in the corresponding Internet Protocol address prefix.

6. The router of claim 5, wherein among the codes corresponding to matching Internet Protocol address prefixes, a code indicating a highest number of relevant bits indicates the longest matching Internet Protocol address prefix.

7. The router of claim 5, wherein the code indicates up to 32 relevant bits in the corresponding Internet Protocol address prefix.

8. The router of claim 5, wherein the code indicates up to 128 relevant bits in the corresponding Internet Protocol address prefix.

9. A method for finding a longest matching prefix for an Internet Protocol address, comprising:

storing Internet Protocol address prefixes in a content addressable memory in an order independent of lengths of the Internet Protocol address prefixes; and

comparing codes corresponding to matching Internet Protocol address prefixes in an encoder to find a longest matching Internet Protocol address prefix.

10. The method of claim 9, wherein the codes indicate numbers of relevant bits in the corresponding Internet Protocol address prefixes.

11. The method of claim 10, wherein among the codes corresponding to matching Internet

Protocol address prefixes, the code indicating a highest number of relevant bits indicates the longest matching Internet Protocol address prefix.

12. A method for generating a router table, comprising:

receiving an Internet Protocol address prefix;

storing the prefix in a router table entry;

generating a code indicating a number of relevant bits in the Internet Protocol address prefix; and

storing the code in the router table entry.

13. A system for reducing a number of multiple matching entries by changing a matching status of one or more less relevant entries in the multiple matching entries to a non–matching status, comprising:

a plurality of entries having one of the matching status and the non–matching status;

a plurality of flags having one of a triggered status and a non–triggered status; and

a plurality of trigger arrays coupled to the plurality of entries and the plurality of flags, wherein each of the plurality of entries is characterized by one of the plurality of trigger arrays.

14. The system of claim 13, wherein each of the plurality of trigger arrays includes:

a plurality of flag triggers having one of a triggering status and a non–triggering status.

15. The system of claim 14, wherein each of the plurality of flag triggers is associated with

one of the plurality of flags, and prompts the associated flag to change to the triggered status if the each of the plurality of flag triggers has the triggering status.

16. The system of claim 15, further comprising:

logic coupled to the plurality of trigger arrays and the plurality of flags, wherein the logic sends a signal prompting one of the plurality of entries to change to the non–matching status if i) an entry the plurality of entries is characterized by a trigger array of the plurality of trigger arrays including a flag trigger of the plurality of flag triggers having the non–triggering status and ii) the flag trigger of the plurality of flag triggers having the non–triggering status is associated with a flag of the plurality of flags having the triggered status.

17. The system of claim 16, wherein a first trigger array of the plurality of trigger arrays characterizing a first entry of the plurality of entries having a greater degree of relevance includes flag triggers of the plurality of flag triggers having the triggering status associated with at least a) every flag of the plurality of flags associated by flag triggers of the plurality of flag triggers having the triggering status included in a second trigger array of the plurality of trigger arrays characterizing a second entry of the plurality of entries having a lesser degree of relevance and b) another flag of the plurality of flags.

18. A circuit for selectively sending a signal to prompt an entry to have a non–matching status, comprising:

a flag having one of a triggered status and a non–triggered status;

a flag trigger coupled to the flag, wherein the flag trigger has one of a triggering status and a non–triggering status, and if the flag trigger has the triggering status, the flag trigger prompts the flag to have the triggered status; and

logic coupled to the flag trigger and the flag, wherein if the flag trigger has the non–triggering status and the flag has the triggered status, then the logic sends the signal to prompt the entry to have the non–matching status.

19. The circuit of claim 18, wherein the flag trigger includes an SRAM, the triggered status is a first binary value, and the non–triggered status is a second binary value.

20. The circuit of claim 18, wherein the flag includes an output of a single–ended sense amplifier, the triggered status is a first output voltage of the single–ended sense amplifier, and the non–triggered status is a second output voltage of the single–ended sense amplifier.

21. The circuit of claim 18, wherein the flag includes a terminal of a transistor, the triggered status is a first output voltage of the terminal of the transistor, and the non–triggered status is a second output voltage of the terminal of the transistor.

22. The circuit of claim 18, wherein the signal prompting the entry to have the non–matching status is sent to a single–ended sense amplifier.

23. The circuit of claim 18, further comprising:

a logic gate coupled to the logic, the logic gate receiving a first signal indicating one of the matching status and the non–matching status of the entry, and a second signal prompting the entry to have the non–matching status.

24. The circuit of claim 18, further comprising:

a find circuitry coupled to the flag trigger, wherein the find circuitry allows the entry to be found for deleting the entry.

25. A method of selectively prompting an entry to have a non–matching status, comprising:

refreshing a flag to have a non–triggered status;

if a flag trigger associated with the flag has a triggering status, prompting the flag to have a triggered status; and

if the flag trigger associated with the flag has a non–triggering status and the flag has a triggered status, prompting the entry characterized by the flag trigger to have the non–matching status.

26. A method of operating a router, comprising:

receiving Internet Protocol address prefixes;

generating codes corresponding to a number of relevant bits in the Internet Protocol address prefix

receiving a packet with a destination Internet Protocol address;

comparing the destination Internet Protocol address to the Internet Protocol address

prefixes to find the Internet Protocol address prefixes that match the destination Internet Protocol address;

comparing the codes corresponding to the matching Internet Protocol address prefixes to find a longest matching Internet Protocol address prefix; and

sending the packet to a port corresponding to the longest matching Internet Protocol address prefix.

27. A method for reducing a number of multiple matching entries by changing a matching status of one or more less relevant entries in the multiple matching entries to a non–matching status, comprising:

defining a plurality of trigger arrays, wherein each trigger array of the plurality of trigger arrays includes a plurality of flag triggers;

characterizing each entry of a plurality of entries with a trigger array of the plurality of trigger arrays;

associating each flag trigger of the plurality of flag triggers with a flag of a plurality of flags;

sending a triggering signal from the flag trigger of the plurality of flag triggers to prompt a flag of the plurality of flags to change to a triggered status, if at least i) the flag trigger of the plurality of flag triggers and the flag of the plurality of flags are associated and ii) the flag trigger of the plurality of flag triggers has a triggering status; and

sending a signal prompting an entry of the plurality of entries to change to the non–matching status if i) the entry of the plurality of entries is characterized by a flag trigger of the

plurality of flag triggers having a non–triggering status, and ii) the flag trigger having the non–triggering status and the flag of the plurality of flags having the triggered status are associated.

28. The method of claim 27, wherein an entry of the plurality of entries having a greater degree of relevance is characterized by a trigger array including more flag triggers having the triggering status and an entry of the plurality of entries having lesser degree of relevance is characterized by a trigger array including fewer flag triggers having the triggering status.

29. The method of claim 28, further comprising:

after sending signals prompting entries of the plurality of entries to change to the non–matching status, determining an only entry having the matching status as a most relevant entry.

30. The method of claim 29, wherein the most relevant entry is an Internet Protocol address prefix determined to be the longest matching prefix.